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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/360,472	07/23/1999	RETO STAMM	X-528-US	4229

24309 7590 04/24/2003

XILINX, INC
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EXAMINER	
PHAN, THAI Q	
ART UNIT	PAPER NUMBER
2123	13

DATE MAILED: 04/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/360,472	Applicant(s) Stamm et al.
	Examiner Thai Phan	Art Unit 2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Feb 6, 2003*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-20* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Oct. 25, 1999* is/are a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Arguments

1. In view of the appeal brief filed on Feb. 06, 2003, PROSECUTION IS HEREBY REOPENED. A new ground of rejection set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

SAMUEL BRODA, ESQ.
PRIMARY EXAMINER

DETAILED ACTION

This Office action is in response to appeal brief, filed on Feb. 06, 2003. Following is the examiner's new ground of rejection. Claims 1-20 are pending in this official action.

Drawings

2. The drawings filed on Oct. 25, 1999 are formally accepted.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollander, US patent no. 6,530,054 B2, in view of Goslin et al., US patent no. 6,120,549.

As per claim 1, Hollander discloses method and apparatus for test generation during circuit design with feature limitations substantially similar to the claimed invention (Abstract). According to Hollander, the test method to verify the device under test includes steps of

randomly generating a set of parameter values for the device under test (col. 2, lines 54-65, col. 5, lines 1-9, col. 7, lines 26-40),

generating a netlist or RTL model from the set of randomly generated parameter values and device under test for verification (col. 13, lines 30-49, for example),

and verifying or simulating circuit behavior with the RTL model or net list as claimed.

Hollander does not expressly disclose parameterizing logic core in the design circuit as claimed. Such feature is well-known in the art. In fact, Goslin teaches method and system for designing integrated circuit with parameterized logic cores (Summary of the Invention, col. 4, line 45 to col. 5, line 23, col. 8, lines 15-60, for example) in order to provide a performance requirement of the design and meet design simulation with minimum simulation time as taught in Goslin, col. 1, lines 51-65.

Practitioner in the art at the time of the invention was made would have found it obvious to combine Goslin teaching of parameterized logic functional block or module in the design into Hollander for the circuit design under testing or simulation to minimize design verification time.

As per claim 2, Goslin teaches upper and lower limits associated with random parameter values (col. 6, lines 48-62, for example), and generating a new random parameter set for the design to meet design specification (col. 7, line 52 to col. 8, line 10).

As per claim 3, Goslin teaches weight file or probability function for parameter values generation in order to randomly generating parameter values (col. 9, line 20 to col. 10, line 14).

As per claim 4, Goslin teaches generating parameter values as input to a graphical user interface (col. 4, lines 26-43, col. 6, line 48 to col. 7, line 25), and replacement values for invalid parameter values to meet design requirement (col. 8, lines 15-60).

As per claim 5, Goslin teaches graphical user interface with feature limitations as claimed to allow user interactive with the design process (cols. 6-8).

As per claims 6 and 7, Goslin teaches generating replacement parameter values for the invalid parameters (col. 8, lines 15-60), and repeating such step for all parameters to meet design requirement.

As per claims 8-9, Goslin teaches parameters fitting and selection as in col. 8, lines 15-60, col. 9, lines 20-51, and col. 10, lines 25-40 could obviously imply the claimed limitations of parameter mutation and cloning for optimizing the circuit verification performance.

As per claim 10, in addition to fitting and selecting parameters for the design verification, Goslin also teaches generating a netlist for the new select set of parameter and simulation of the new netlist as claimed (col. 8, lines 4-10, and lines 15-60, and col. 9, lines 20-51).

As per claims 11-14, Goslin teaches design parameters selection and fitting which would obviously imply the claimed limitations in order to improve performance verification (col. 9, lines 20-51, col. 10, lines 25-40).

As per claim 15, Goslin teaches graphic user interface and interactive means to allow user to key in design parameters selection, change, or set as claimed (col. 4, lines 26-43, col. 6, line 48 to col. 7, line 25).

As per claim 16, Goslin teaches design order in order to generating parameters for the design, and generating parameter values for the orderly hierarchy of the design process (col. 5, lines 23-65, col. 6, lines 1-18, for example).

As per claim 17, Goslin teaches design verification including performance a number of design simulation, accumulating of fail test data, recording parameters of the design simulation, etc. in order to verify the design performance.

As per claim 18, Hollander discloses method and apparatus for test generation during circuit design with feature limitations substantially similar to the claimed invention (Abstract). According to Hollander, the test apparatus to verify the device under test includes means

test controller for randomly generating a set of parameter values for the device under test (col. 2, lines 54-65, col. 5, lines 1-9, col. 7, lines 26-40),

means for generating a netlist or RTL model from the set of randomly generated parameter values and device under test for verification (col. 13, lines 30-49, for example),

and means for verifying or simulating circuit behavior with the RTL model or net list as claimed.

Hollander does not expressly disclose parameterizing logic core in the design circuit as claimed. Such feature is well-known in the art. In fact, Goslin teaches method and system for designing integrated circuit with parameterized logic cores (Summary of the Invention, col. 4, line 45 to col. 5, line 23, col. 8, lines 15-60, for example) in order to provide a performance requirement of the design and meet design simulation with minimum simulation time as taught in Goslin, col. 1, lines 51-65.

Practitioner in the art at the time of the invention was made would have found it obvious to combine Goslin teaching of parameterized logic functional block or module in the design into Hollander for the circuit design under testing or simulation to minimize design verification time.

As per claim 19, Hollander discloses method and apparatus for test generation during circuit design with feature limitations substantially similar to the claimed invention (Abstract). According to Hollander, the test method to verify the device under test includes means to provide method of testing device under test:

means with graphical user interface for randomly generating a set of parameter values for the device under test (col. 2, lines 54-65, col. 5, lines 1-9, col. 7, lines 26-40),

means for generating a netlist or RTL model from the set of randomly generated parameter values and device under test for verification (col. 13, lines 30-49, for example),

and verifying or simulating circuit behavior with the RTL model or net list as claimed.

Hollander does not expressly disclose parameterizing logic cores and means for generating such cores in the design circuit as claimed. Such feature is well-known in the art. In fact, Goslin teaches method and system for designing integrated circuit with parameterized logic cores (Summary of the Invention, col. 4, line 45 to col. 5, line 23, col. 8, lines 15-60, for example) in order to provide a performance requirement of the design and meet design simulation with minimum simulation time as taught in Goslin, col. 1, lines 51-65.

Practitioner in the art at the time of the invention was made would have found it obvious to combine Goslin teaching of parameterized logic functional block or module in the design into Hollander for the circuit design under testing or simulation to minimize design verification time.

As per claim 20, Hollander discloses method and apparatus for test generation during circuit design with feature limitations substantially similar to the claimed invention (Abstract). According to Hollander, the test apparatus to verify the device under test includes means

test controller for randomly generating a set of parameter values for the device under test (col. 2, lines 54-65, col. 5, lines 1-9, col. 7, lines 26-40),

means for generating a netlist or RTL model from the set of randomly generated parameter values and device under test for verification (col. 13, lines 30-49, for example),

and means for verifying or simulating circuit behavior with the RTL model or net list as claimed.

Hollander does not expressly disclose parameterizing logic core in the design circuit as claimed. Such feature is well-known in the art. In fact, Goslin teaches method and system for designing integrated circuit with parameterized logic cores (Summary of the Invention, col. 4, line 45 to col. 5, line 23, col. 8, lines 15-60, for example) in order to provide a performance requirement of the design and meet design simulation with minimum simulation time as taught in Goslin, col. 1, lines 51-65.

Practitioner in the art at the time of the invention was made would have found it obvious to combine Goslin teaching of parameterized logic functional block or module in the design into Hollander for the circuit design under testing or simulation to minimize design verification time.

Response to Arguments

5. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 6,463,560 B1, issued to Bhawmik et al., on Oct. 2002

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this action should be mailed to:
Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:
(703) 746-7239, (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

April 21, 2003

Thai Phan
Patent Examiner
AU 2123